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PERFORMANCE ANALYSIS OF SIMPLIFIED SILICON SOLAR CELL ON *P*-TYPE CRYSTALLINE SILICON WAFER

(Analisis Prestasi Bagi Sel Suria Silikon Teringkas Ke Atas Silikon Wafer Kristal Jenis-*P*)

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Abstract

Crystalline silicon (c-Si) wafers are the dominating substrate materials for solar cells in current photovoltaic (PV) industry. Silicon (Si) wafer with positive-type (*p*-type) based solar cells dominates almost 95% of the global PV market. Recent goal in Si solar cell industry is focusing on cost reduction through inexpensive manufacturing processes. Standard manufacturing process of Si solar cell fabrication consist of damage removal, cleaning, texturing, phosphorus oxytrichloride ($POCl_3$) diffusion, anti-reflective coating (ARC) deposition, metallization by screen printing technique, firing and light current-voltage (LIV) testing. These fabrications line are time–consuming and high temperature process which lead to high manufacturing cost. This study presents the simplification of Si solar cell fabrication on *p*-type Si wafer. Simplified fabrication process eliminates the ARC deposition by plasma enhanced chemical vapour deposition (PECVD). Simplified Si solar cell was fabricated without silicon nitride (SiN) as ARC layer. In commercial solar cell, both pyramid texture on Si wafer and SiN have been used to reduce reflectance and enhanced the light absorption. From the reflectance measurement, it can be seen that SiN and pyramid texture shows an average reflectance curve. The efficiency obtained by commercial, fabricated and simulated solar cells were 17.09%, 9.44% and 9.67%, respectively. From the simulation study, it is proven that the low efficiency of simplified solar cell was attributed by low minority carrier lifetime of *p*-type Si wafer.

Keywords: crystalline silicon solar cell, *p*-type Si wafer, anti-reflective coating, minority carrier life time, PC1D simulation

Abstrak

Kepingan silikon kristal (c-Si) adalah bahan substrat yang mendominasi sel suria untuk industri fotovolta (PV) masa kini. Sel suria berasaskan kepingan silikon (Si) berjenis-*p* menguasai hampir 95% daripada pasaran PV global. Matlamat terkini dalam industri sel suria Si memfokuskan kepada pengurangan kos melalui proses pembuatan yang murah. Piawai pembuatan fabrikasi sel suria Si terdiri daripada penyingkiran kotoran, pembersihan, pentekstur an, penyerapan fosforus oksitriklorida ($POCl_3$), pemendapan lapisan anti-pantulan (ARC), penyaduran dengan teknik percetakan skrin, pembakaran dan ujian cahaya arus-voltan (LIV). Proses fabrikasi piawai ini memakan masa dan menggunakan suhu tinggi yang menyebabkan kos pengeluaran yang tinggi. Kajian ini membentangkan peringkasan proses fabrikasi sel suria Si di atas Si wafer jenis-*p*. Proses fabrikasi teringkas ini membuang proses pemendapan ARC oleh pengendapan kimia dipertingkat plasma (PECVD). Sel suria Si teringkas telah difabrikasi tanpa lapisan silikon nitrida (SiN) sebagai ARC. Dalam sel suria komersial, tekstur piramid pada Si wafer dan SiN telah digunakan untuk mengurangkan pantulan dan meningkatkan penyerapan cahaya. Dari pengukuran pantulan, SiN dan tekstur piramid menunjukkan pantulan yang agak sama. Kecekapan yang diperolehi oleh sel suria komersial, diringkas dan simulasi adalah masing-masing pada 17.09%, 9.44% dan 9.67%. Daripada kajian simulasi, ia membuktikan bahawa kecekapan yang rendah bagi sel suria teringkas adalah disebabkan oleh jangka hayat pembawa minoriti yang rendah pada Si wafer jenis-*p*.

Kata kunci: kristal silikon sel suria, kepingan silikon jenis-*p*, lapisan anti-pantulan, jangka hayat pembawa minoriti, simulasi PCID

Introduction

Solar cell is a semiconductor device which converts sunlight into electricity. Silicon (Si) is the most developed and widely used element in manufacturing solar cells. It is an indirect bandgap semiconductor and can be doped by impurities such as boron or phosphorus to form highly conductive positive or negative regions. It also absorbs light over a broad spectral range from ultra-violet (UV) to near infra-red (NIR) range. Si is a non-toxic material and the second most abundant element (after oxygen) on earth with a concentration of 28% [1]. The Si solar cell essentially has three functional elements: (a) absorption of sunlight to form electron-hole ($\bar{e}$-h) generation pairs, (b) an internal electric field (p-n junction) to separate $\bar{e}$-h pairs, and (c) external electrical contacts to extract current [2]. The Si wafer itself acts as the light absorber to generate $\bar{e}$-h pairs. The junction inside the semiconductor prevents $\bar{e}$-h pairs from recombination and guides oppositely charged carriers to respective electrical contacts. Finally, the contacts act as wires to carry photo-generated current into a load. Market review reveals that p-type wafer based solar cell dominates almost 95 % of the worldwide PV market [3].

Figure 1(a) shows the standard manufacturing process in solar cell fabrication that consist of damage removal, texturing, junction formation by phosphorus oxytrichloride ($POCl_3$) diffusion, Silicon nitride (SiN) deposition as ARC, metallization by screen printing technique, firing and IV testing. SiN is widely used as ARC layer in commercial c-Si solar cell deposited by PECVD. ARC deposition and diffusion processes consumed 50% to 70% energy from total energy consumption in solar cells fabrication process [4]. In addition, SiN uses silane toxic gas while $POCl_3$ diffusion requires temperature of 1000 °C for junction formation. High temperature process leads to high fabrication cost, meanwhile SiN deposition is a toxic-based process. Therefore, this study presents simplified fabrication process for c-Si solar cell on p-type wafers. This process eliminates the use of SiN as ARC layer (Figure 1(b)). Previous study has presented the *in-situ* oxidation process of silicon dioxide (SiO_2) as ARC layer [5]. However, in this paper, we presented performance evaluation of Si solar cell without ARC layer by experiment and PC1D simulation. Solar cell simulation model PC1D is used to understand dependence of solar cell performance on wafer and process parameters.

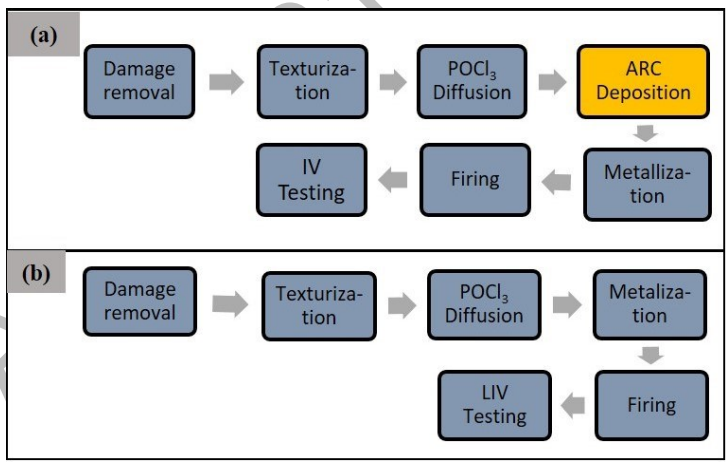

Figure 1. Comparison of (a) standard manufacturing process for Si solar cell fabrication, and (b) fabrication process for simplified Si solar cell on p-type Si wafer. There is an elimination of ARC deposition process in simplified Si solar cell

Materials and Methods

Fabrication of simplified *p*-type Si solar cell

Figure 2(a) schematically describes the commercial solar cell configuration, meanwhile Figure 2(b) describes simplified solar cell configuration without ARC layer. The saw damage in as-cut boron wafers was removed by etching in 10% sodium hydroxide (NaOH) solution. A mixture of 6000 ml deionized (DI) water and 600 g of NaOH

was prepared in Pyrex beaker and the solution was heated to 70 ^{o}C. Si wafers were fully immersed into heated solution for 10 minutes. This process removes surface saw damage and other contaminants from the wafering process. The etched wafers are rinsed in DI water and immersed in dilute hydrofluoric (HF) solution to remove native oxide. Appropriately processed wafers will exhibit shiny surface and are completely hydrophobic. An alkaline solution is highly effective in creating a uniform texture for the texturing process on <100> crystalline orientation. A mixture of isopropyl alcohol:potassium hydroxide:deionized water (IPA:KOH:H_2O) was prepared based on volume ratio 5:1:123. The solution was heated up at 70 ^{o}C. The saw-damage removed wafers are immersed in this solution for 30 minutes. Finally, the wafer is rinsed in DI water and immersion in 10% HF solution. With appropriate texture process, surface appearance is grey and shiny at large oblique angles due to high reflection of <111> crystalline facets. Such rough surfaces enhance light trapping and reduce reflection.

A *p-n* junction is formed based phosphorous diffusion with liquid source $POCl_3$ solution. A vapour solution containing $POCl_3$ is transported to a high temperature quartz furnace to form Phosphorous Oxide film on the Si wafer surface. Next, the metallic pastes were screen printed on both the front and rear surfaces of the Si wafer. At the front, Ag paste is screen printed and dried in low temperature oven at 200 ºC for 10 minutes. Following front surface screen printing, rear surface is screen printed by with an Al paste and dried in low temperature oven at 200 ºC for 10 minutes. The drying process removes excess organic solvent from the pastes and provides stable adhesion between paste and wafer surfaces. The aim of this process is to form low resistance ohmic contacts between metallic films and Si. In this process, wafers were placed on the top of the conveyer belt and passes through six temperature zones. Each of temperature zones is heated up by infrared quartz lamps. The finished solar cells were characterized by light current-voltage (LIV) measurement system and quantum efficiency (QE) measurement systems using Keithley 237.

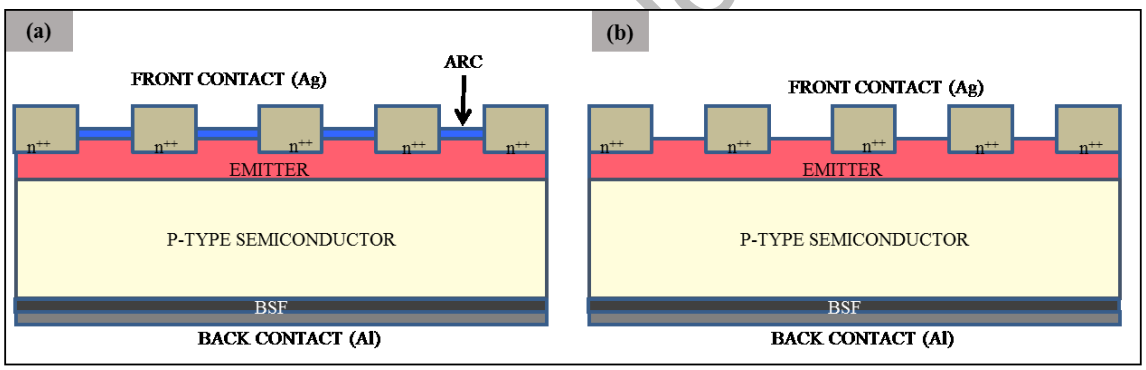

Figure 2. Schematic diagram for device configuration of (a) commercial p-type Si solar cell; and (b) simplified *p*-type Si solar cell

PC1D simulations of simplified *p*-type Si solar cell

PC1D simulation software was used to simulate performance of *p*-doped wafer solar cell in terms of critical solar cell parameters such as bulk conductivity, front surface field and minority carrier lifetime [6]. Figure 2 described the differences schematic configuration between (a) ARC and (b) non-ARC solar cell configuration. Non-ARC simulation was carried out for 100 cm^2 area p type silicon solar cell with fixed series resistance, shunt conductance, and 200-μm wafer thickness. Pyramidal texture was assumed with fixed 10 % front surface reflectance. Base contact and internal conductor were respectively set at 0.0015 Ω and 0.3 S [7]. Bulk conductivity concentrations were varied in $1.513\times10^{11}/cm^3$ to $1.513\times10^{16}/cm^3$ range. The front surface emitter doping concentration was varied from $1.27\times10^{17}/cm^3$ to $1.27\times10^{22}/cm^3$. The minority carrier lifetime was varied from 0.001 μs to 1000 μs. Finally, the front surface recombination velocity was varied in 1×10^{6} cm/s to 100 cm/s. Table 1 shows the details of simulation parameters.

Table 1. Simplied Si solar cell parameters in PC1D simulation

Parameters	**Value and Unit**
Device area	100 cm^2
Front surface texture depth	3 μm/ 54.74°
Rear surface texture depth	3 μm/ 54.74°
Front / Rear surface coating enabled	Yes
Internal / external optical reflectance	10%
Base contact	0.015 Ω
Internal conductor	0.3 S
Thickness	200 μm
Material	Silicon (Si)
Carrier mobilities for electron and holes (μ_e /μ_h)	1450 cm^2/Vs 413 cm^2/Vs
Dielectric constant	11.9
Band gap	1.124 eV
Intrinsic conc. At 300K	1×10^{10} cm^{-3}
Absorption coefficient	Silicon
Free carrier absorption enabled	Yes
P-type background doping	1.513×10^{16} cm^{-3}
1st front diffusion: *n*-type	1×10^{17} cm^{-3}
2nd front diffusion	-
1st rear diffusion: *p*-type	1×10^{19} cm^{-3}
Bulk recombination	0.1 μs
Front surface recombination	10 cm/s
Rear surface recombination	10 cm/s
Temperature	25°C
Base circuit	-0.8 to 0.8 V
Collector circuit	Zero

Results and Discussion

The investigation on reflectance measurement has been performed to investigate the photon reflection of pyramid texture Si wafer and SiN as ARC layer. Scanning electron microscopy (SEM) images of pyramid textured and ~70 nm thin SiN layer on Si wafer shown in Figure 3(a) and Figure 3(b). In commercial solar cell, both pyramid texture and SiN layer have been used to reduce light reflectance and enhanced photon absorption. Figure 4 shows the reflectance measurement of planar (un-textured) wafer, textured wafer and SiN layer on Si wafer. The high reflectance shown by planar wafer indicates that the light is highly reflected on un-textured and non-ARC wafer. Therefore, the planar wafer is not appropriate in Si solar cell fabrication as it has high photon and reflection losses. Meanwhile, textured wafer and SiN layer shows an average performance on reflectance measurement. This average performance of the reflectance measurement proves that non-ARC Si solar cell can potentially produce a good performance output of solar cell compared to commercial solar cell.

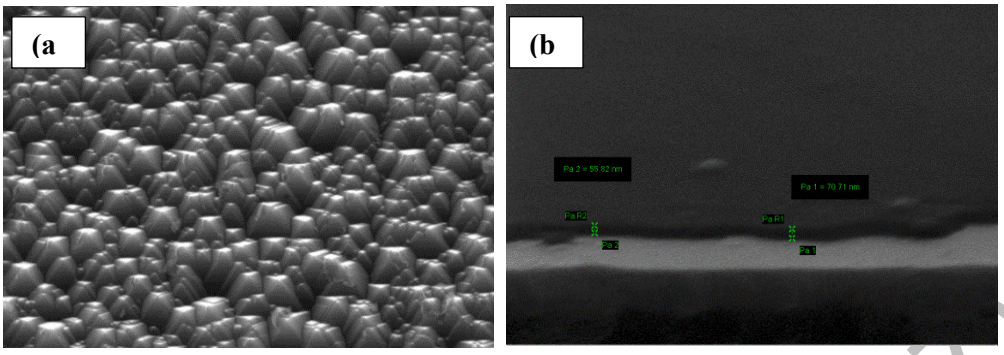

Figure 3. SEM images of (a) pyramid texture on Si wafer, and (b) SiN layer as ARC on commercial Si solar cell

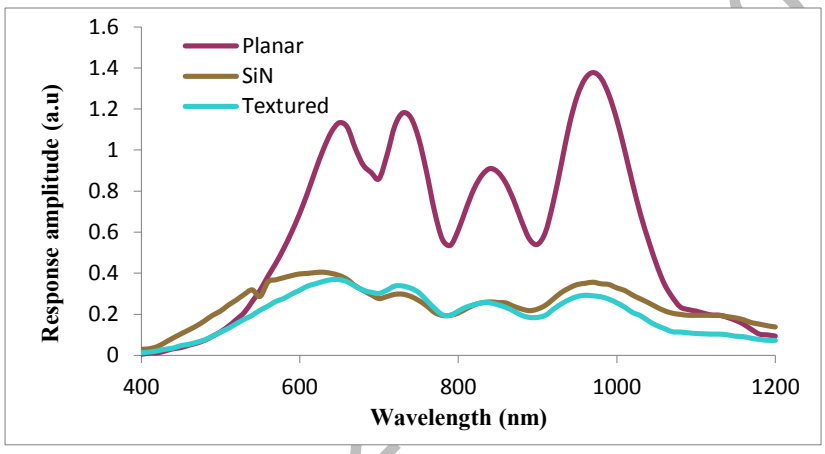

Figure 4. Reflectance measurement on planar wafer, textured wafer and SiN layer on Si wafer

Figure 5 plots current-voltage (I-V) measurements at air mass (AM) 1.5 illumination for commercial solar cell, fabricated and simulated simplified Si solar cell on *p*-type Si wafer. Table 2 summarizes the solar cells performances. In Figure 5, the commercial solar cell as reference cell exhibits significantly superior performance in comparison with simplified solar cell. The efficiency obtained by commercial, fabricated and simulated solar cells were 17.09%, 9.44% and 9.67%, respectively. The commercial solar cell has textured Si wafer and SiN layer as ARC, while fabricated simplified solar cell is non-ARC solar cell and textured. It can be seen that there is a sub-standard performance between commercial and non-ARC solar cell with ~8% of difference in solar cell efficiency. This proves that non-ARC solar cell can still produce a function solar cell without SiN layer. These findings raise up an approach to have the non-toxic solar cell at low fabrication cost.

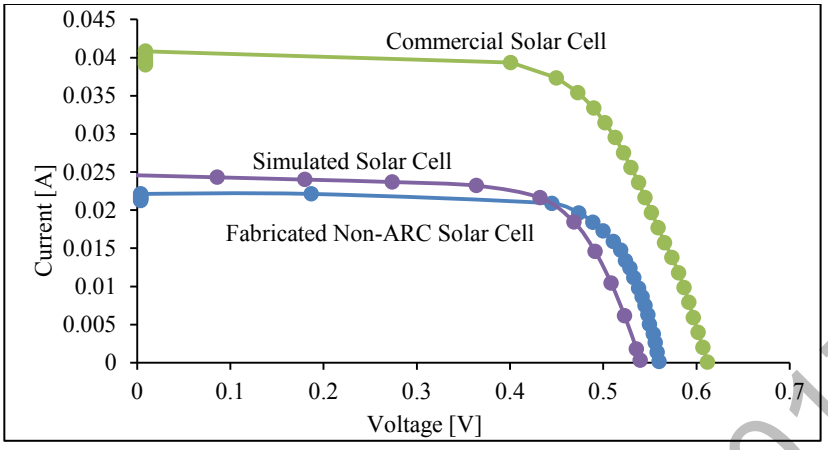

Figure 5. I-V curve of commercial, simulated and fabricated solar cell under AM 1.5 illumination

Table 2. Solar cell performances of commercial, fabricated and simulation solar cell

Device Performances	**Commercial Solar Cell**	**Fabricated Solar Cells**	**Simulated Solar Cell**
Voc (V)	0.612	0.56	0.50
Isc [A]	0.041	0.02	0.025
FF	0.671	0.7467	0.724
Efficiency (%)	17.09	9.44	9.67

The minority carrier lifetime of *p*-type Si wafer has been varied in PC1D simulation at 0.15 μs, 0.6 μs and 1.1 μs to investigate the significance of the lifetime to the simplified solar cells performance. The lack performance of fabricated simplified solar cell can be attributed to the relatively poor minority carrier lifetimes of *p*-type Si wafers. Figure 6 shows minority carrier lifetime at 0.15 μs, 0.6µs and 1.1 μs resulting solar cell efficiency of 10.34%, 12.30% and 13.03% respectively. This result indicated that the front surface emitter field is able to collect large majority light-generated $\bar{e}$-*h* pairs prior to recombination. However, poor lifetime means that a majority of $\bar{e}$-*h* pairs are lost to recombination prior to collection by the junction. *I-V* curve in Figure 5 and 6 shows a good agreement.

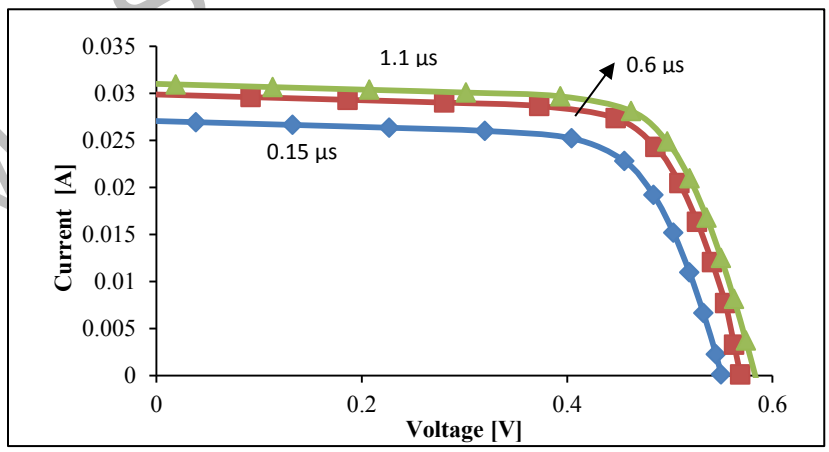

Figure 6. *I-V* response of simulated simplified solar cell with a variation of minority carrier lifetime at 0.15 μs, 0.6 μs and 1.1 μs by PC1D simulation

In addition, this behaviour can be explained in terms of electron-hole pair diffusion across the 200 μm thickness of the solar cell. Diffusion length is related to lifetime by the equation (1).

$$L_{DIFF} = (\tau * D)^{1/2} \quad (1)$$

where τ is minority carrier lifetime in second and D is Si diffusivity in m^2/sec; for Si, $D=8.8\times10^{-5}$ m^2/sec. Therefore, for τ=0.001 μs, L_{DIFF}=0.3 μm which is 667 times smaller than wafer thickness; therefore, almost all $\bar{e}$-h pairs are likely to be lost to recombination. In contrast, for τ=500 μs, L_{DIFF}=210 μm, which is larger than wafer thickness; therefore, almost all $\bar{e}$-h pairs will likely reach junction prior to recombination [7]. Ergo, higher efficiency of simplified solar cell can be achieved by using higher minority carrier lifetime of Si wafer. Higher lifetime wafers can produce an average performance of simplified solar cell similar as commercial solar cell that has SiN layer.

Conclusion

Simplified Si solar cells or non-ARC solar cell have been fabricated and modelled in PC1D. The efficiency obtained by fabricated and simulated solar cells were 9.44% and 9.67%, respectively. The commercial solar cell with ARC layer shows an efficiency of 17.09%. Good agreement is observed between the experimental and simulation results. The low efficiency of the fabricated solar cell has been attributed to the no ARC layer and poor minority carrier lifetime of Si wafer. However, the efficiency of simplified solar cell and the reflectance measurements shows that non-ARC Si solar cell potentially produce an average performance output of solar cell compared to commercial solar cell. Therefore, high minority carrier lifetime is required in order to produce high efficiency of simplified solar cell. This work also contributes to the simple approach of solar cell fabrication at low cost.

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