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PERFORMANCE OF ORGANIC THIN FILM TRANSISTORS (OTFTs) AT VARIOUS TEMPERATURES ON POLYETHYLENE TEREPHTHALATE (PET) SUBSTRATE

(Prestasi Transistor Organik Filem Nipis (OTFTs) pada Suhu yang Berbeza di atas Substrat Polietilena Tereftalat (PET)

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Abstract

Fabrication of organic thin film transistors (OTFTs) on a flexible substrate has been the subject of much attention in the sensor research community as its cost effective, low temperature processing, ease of fabrication, disposability and delivery of accurate result. The OTFTs with pentacene as active layer and polymethyl methacrylate (PMMA) as gate insulator was fabricated and its performance was investigated. The PMMA and pentacene thin films were coated on indium tin oxide coated polyethylene terephthalate (PET) substrate by a spin coating method. The substrates temperature were varied at 40, 60, 80 and 100 ^{o}C prior to the deposition of aluminum onto the interdigitated electrodes (IDE) structure via physical vapour deposition (PVD) method. The atomic force microscopy (AFM) images and current-voltage (I-V) relationship indicated that the variation of substrate temperature has an impact on both physical and electrical properties of pentacene thin film transistors. The AFM images show that the morphological grain size increased as the substrate temperature was increased. In addition, the I-V measurement using SPA shown that the source-drain current of OTFTs was highest at temperature 100 ^{o}C.

Keywords: Organic Thin Film Transistors (OTFTs), pentacene, Polyethylene Terephthalate (PET) substrate, Polymethyl Methacrylate (PMMA)

Abstrak

Fabrikasi transistor organik filem nipis (OTFTs) di atas substrat fleksibel telah menjadi perhatian dalam komuniti penyelidikan sensor kerana berkos sederhana, suhu pemprosesan rendah, mudah difabrikasi, pakai buang dan memberikan keputusan yang tepat. OTFTs dengan mnggunakan pentasina sebagai lapisan aktif dan polimetil metakrilat (PMMA) sebagai pintu penebat telah difabrikasi dan prestasinya dikaji. PMMA dan filem nipis pentasina disediakan di atas substrat indium timah oksida bersalut polietilena tereftalat (PET) melalui kaedah salutan putaran dan suhu permukaan dipelbagaikan pada 40, 60, 80 dan 100 ^{o}C sebelum elektod interdigitated (IDE) aluminium dihasilkan melalui kaedah pemendapan wap fizikal (PVD) pada substrat. Gambar daya mikroskop daya atom (AFM) dan hubungan voltan semasa (I-V) telah menunjukkan bahawa suhu teleh memberi impak terhadap sifat fizikal dan elektrik transistor filem nipis pentasina tersebut. Gambar AFM menunjukkan bahawa saiz

butiran morfologi bertambah apabila suhu permukaan meningkat. Di samping itu, ukuran I-V menggunakan SPA menunjukkan bahawa arus punca-saliran OTFTs adalah tinggi pada suhu 100 ^{o}C.

Kata kunci: Organik filem nipis (OTFTs), pentasina, Substrat Polietilena Tereftalat (PET), Polymetil Metakrilat (PMMA)

Introduction

Organic thin film transistors (OTFTs) have been popular in the research community due to its potential to be cost effective [1], low temperature processing [2], ease of fabrication, disposability and delivery of accurate results. The OTFTs consist of three terminals that are the source, drain and gate that allows controlling current flow between the two electrodes through the modulation of the voltage at the third electrode [3]. Most of OTFTs prepared by vacuum deposition technique showed better electrical performances on the silicon-based thin film transistors (TFTs). However, this technique has limitation for the large area application, so a new technique has been proposed using solution process [4].

Among the various organic semiconductors that are being considered as the active materials in OTFTs, pentacene is one of the most promising and widely used due to its outstanding performance in terms of electrical performance such as mobility, threshold voltage and on-off ratio [5]. Therefore, pentacene is the best candidate for the p-type semiconductor OTFT. Its advantages also include air stability and good solubility. The face-to-face stacking in crystalline form is very beneficial for Π-orbital overlap [6].

In this research, pentacene, used as the active material for OTFTs was deposited at 40, 60, 80 and 100 ^{o}C and the electrical performance was investigated by I-V measurement using semiconductor parameter analyzer (SPA). The morphology of pentacene on polyethylene terephthalate (PET) substrate at various temperatures was investigated using an atomic force microscope (AFM).

Materials and Methods

Materials and Chemicals

Anisole, Decane, Polymethyl methacrylate (PMMA), 6, 13- Bis(triisopropylsilylethynl) pentacene, aluminum wire and indium tin oxide coated polyethylene terephthalate (PET) substrate were purchased from Sigma Aldrich.

Organic Thin Film Transistors (OTFTs) Fabrication

The TIPS-pentacene based OTFTs were fabricated in a top contact and bottom gate structure, as shown in Figure 1. The Indium tin oxide (ITO) layer on the PET substrate was patterned for a gate electrode.

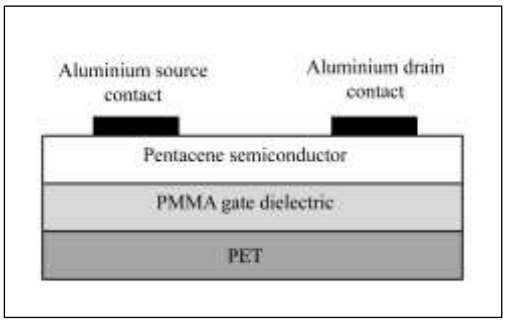

Figure 1. Schematic Structure of OTFT Device on PET Substrate

The thin films of pentacene were deposited on the PET substrates having the dimension of 2” x 2”. Before fabrication process, the substrate was cleaned and kept at ambient temperature. The Polymethyl methacrylate (PMMA) was spin coated on the cleaned substrates at 600 rpm for 60 s to form a gate insulator. The PMMA,

molecular weight of 120 K was diluted in anisole (4 wt %). The spin coated PMMA was baked at 40, 60, 80 and 100 ^{o}C for 60s. For an organic semiconductor, TIPS-pentacene which is dissolved in 91 % anisole and 9 % decane by weight, was spin coated onto the PMMA gate insulator at 600 rpm for 60 s and baked at 40, 60, 80 and 100 ^{o}C for 60 s on a hot plate. The source and drain electrodes, aluminium layer were deposited through the shadow mask by using physical vapour deposition (PVD). The pentacene TFTs have a device length (L) and width (W) dimensions of 5.0 mm and 10.0 mm, respectively. Figure 2 shows an OTFT fabricated on Indium tin oxide coated PET substrate.

The surface morphology of pentacene thin film was obtained using atomic force microscopy (AFM) with contact mode and 5 x 5 μm^2 were scanned. The electrical measurements were performed using semiconductor parameter analyzer (Keithley 4200).

Figure 2. OTFT Fabricated On Indium Tin Oxide Coated PET Substrate

Results and Discussion

The surface morphology of pentacene thin film deposited at temperatures of 40, 60, 80 and 100 ^{o}C were obtained using AFM. The information about the effect of varying substrate temperatures can be gained by looking at the AFM images of pentacene layer of different samples in Fig. 3(a – d) which are for to 40, 60, 80 and 100 ^{o}C, respectively. Figure 3 shows AFM images of the pentacene thin films on PET substrates with an area of 5 × 5 μm^2. According to Figure 3, the morphological grain size increased as the substrate temperature was increasing. The grain size obtained at 100 ^{o}C film is larger than that at 40 ^{o}C. This is because by increasing substrate temperatures, the mobility of the molecule to arrive at the surface increases. Thus, produce a better alignment of the molecules and lower nucleation density [1].

The surface roughness of pentacene thin films increased from 0.84 to 10.60 nm as the temperature increased from 40 to 100 ^{o}C. As the surface roughness increased, the root mean square (RMS) roughness also increased as shown in Figure 4. This is because the nucleation and grain structure of pentacene are very sensitive to the changes in substrate temperature. According to Chanhom and Nukeaw [7], the higher temperature would cause increasing of the grain size by restructuring of pentacene molecule as seen in the AFM results (Figure 3). The modification in the pentacene molecule structure gives effect towards the surface grain morphology of pentacene. This is due to the weaker interaction between impinging molecules and the surface [8].

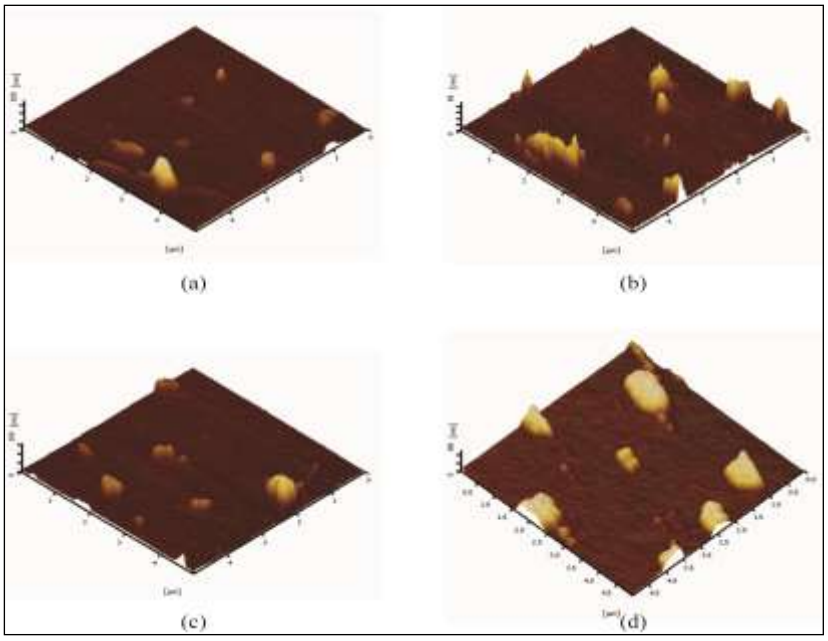

Figure 3. Pentacene OTFTs deposited at T_{sub} of (a) 40 ^{o}C, (b) 60 ^{o}C, (c) 80 ^{o}C and (d) 100 ^{o}C

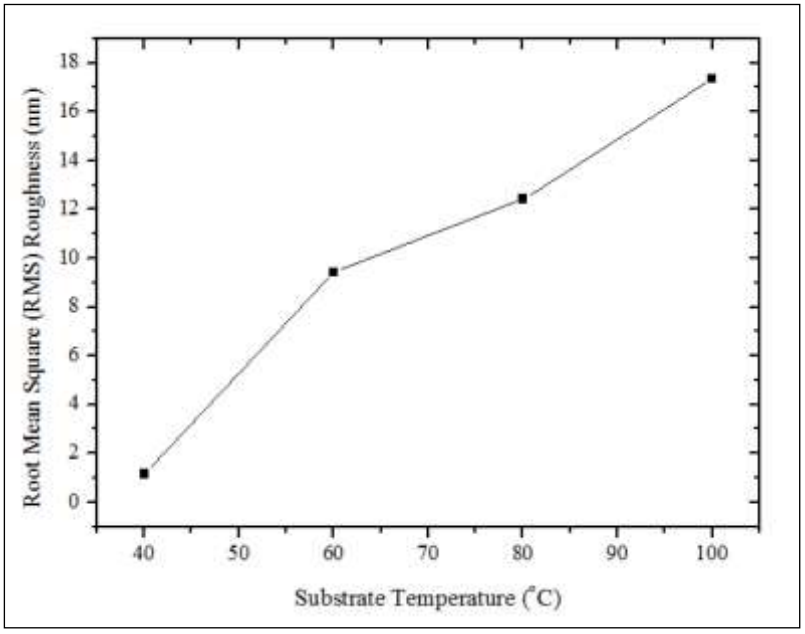

Figure 4. The Root Mean Square (RMS) Roughness of Pentacene Thin Film Proportion to Substrate Temperature

The surface roughness and RMS roughness of pentacene thin film has a significant influence on the device performance. Thus, measuring the surface roughness and RMS roughness are important before manufacturing the device. Current-Voltage (I-V) for OTFTs is shown in Figure 5. The I-V plots display the drain-source current (I_{DS}) versus drain-source voltage (V_{DS}) at fixed gate-source voltage (V_{GS}) values. Usually, OTFTs characteristic followed the traditional behavior of FET and showed typical p-type semiconductor. The I-V characters indicate comparable values of drain -source current at various temperature for OTFTs on PET substrate. From this research, it shows that V_{GS} strongly affected the current flow through the OTFTs.

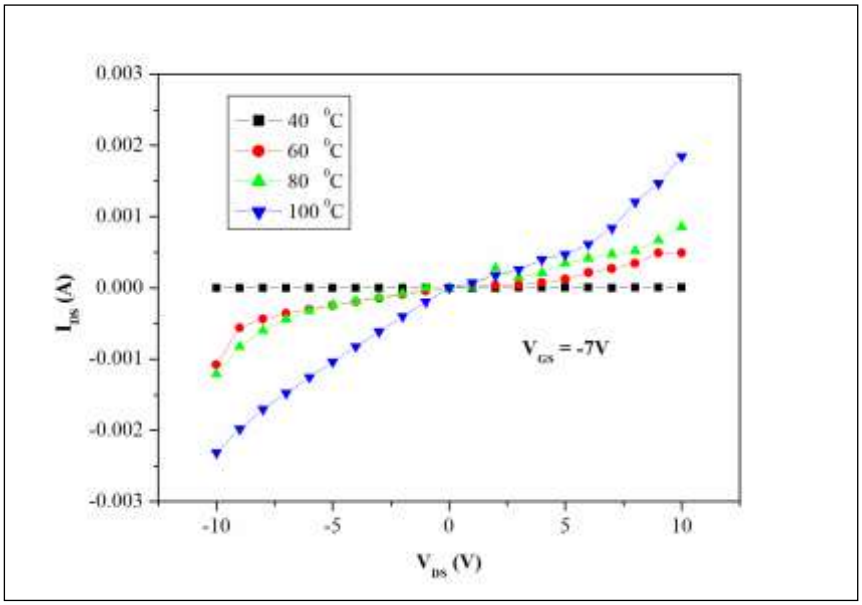

Figure 5. Output Characteristics of Pentacene OTFTs Using PMMA as Gate Insulator at Various Temperatures

I_{DS} was measured by V_{DS} sweeping from -10V to 10V with the swept of 1.0 V step at constant V_{GS}. I_{DS} is higher when a negative voltage is applied at V_{GS}= -7V. For negative gate-source voltage, pentacene OTFTs operate in the accumulation mode and the accumulated charge are holes [9]. During forward biased, electrons are repelled by the external voltage (V_{gs}) applied to the gate transistor and some of the charges are repelled from the area of the gate called depletion region. The highest value 0.00185 A of drain current, I_{DS} of pentacene-OTFTs obtained from pentacene-OTFTs with thin films deposited at T_{sub} = 100^{o}C. Furthermore, the effective carrier mobility when T_{sub} = 100 ^{o}C is larger compared to other OTFTs pentacene with different T_{sub}. It is because when the temperature increase; the grain size increased, thus reducing the grain boundaries. An electron carrier that traps at the grain boundaries decreased by reducing the grain boundaries. This situation will increase the number of effective carriers that leads to higher drain current.

Conclusion

OTFTs based on pentacene active layer and PMMA as dielectric have been fabricated. The temperature dependence of the pentacene OTFTs distinguishes different physical and electrical properties of them. It is found that increasing substrate temperature resulted in the increased grain size and surface roughness. The result also shows that PMMA and pentacene can be easily deposited by spin coating method. From this experiment, the average grain size and RMS roughness of pentacene thin film are largest at T_{sub} = 100^{o}C and its show the highest value of I-V measurement 0.00185 A at T_{sub} = 100^{o}C. This study can be extended to further OTFTs research and useful for chemical and bio sensing materials.

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